A New Overlap-Scan Circuit for High Speed and Low Data Voltage in Plasma-TV

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Abstract — *A new overlap-scan circuit that enables a high speed scan or low data voltage scan based on overlapping the scan pulses during a scan-period is proposed for a 42-in. plasma TV. For the overlap between the scan pulses, the proposed overlap-scan circuit consists of three odd and three even drivers that alternately provide the scan pulses to the odd and even scan lines among the 480 scan lines, respectively. Consequently, the proposed overlap-scan circuit can perform either a high-speed scan by reducing the total scan time or a low voltage scan by lowering the address voltage*[1].

Index Terms — Plasma-TV, high-speed scan, low data voltage scan, overlap-scan circuit, overlap-scan pulse

I. INTRODUCTION

PLASMA-TVs are being acknowledged as the most promising candidate for digital high definition (HD) TV due to such prominent features as a slim-type large area (> 40-in.), self-emitting-based color reproduction capability, wide dynamic contrast ratio, and fast response (few microseconds). However, to capture the TV consumer market and take the lead from LCD-TVs, the cost of a plasma-TV certainly needs to be lowered to a reasonable price [1]. One of the best cost reduction methods is to shorten the address time for single scan driving and lower the address voltage, thereby considerably lowering the cost of the address circuit. As such, various studies have already pursued this area [2], [3]. In a plasma-TV, the scan procedure is carried out line-by-line, where only the wall charges for the displayed cells are accumulated through the address discharge. Fig. 1 shows the scan pulse and corresponding light waveform emitted during the application of the scan pulse, and a certain amount of time is clearly required to produce the address discharge and accumulate the wall charges. In a conventional scan method, the scan pulses between successive scan lines should not overlap to prevent a misfiring discharge. As a result, the total scan time is determined simply by multiplying the time width per scan pulse with the total number of lines. However, as seen in Fig. 1, since no discharge can be produced during the time of T_f, called the formative time lag, if the scan pulses are overlapped only during the formative time lag, no misfiring discharge will be induced [4]. Therefore, this physical phenomenon for the address discharge enables an overlap scanning procedure, as a kind of parallel-pipeline concept.

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Accordingly, this paper proposes a new overlap-scan circuit that enables a high-speed scan or low-data voltage scan by overlapping the scan pulses during an address-period in a 42-in. plasma-TV. The validity of the overlap scan circuit is examined under various image patterns on a 42-in. plasma-TV.

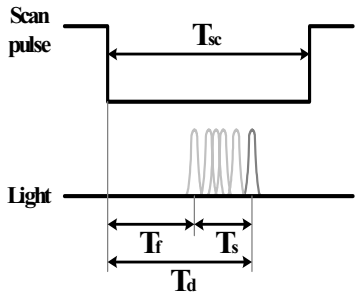

Fig. 1 Scan pulse and corresponding light waveform emitted during address discharge, where T_{sc} is scan pulse width, T_f is formative time lag, and T_s is statistical time lag.

II. EXPERIMENT

Fig. 2 shows a schematic diagram of the back-plate of a 42-in. plasma-TV, which includes the Y-board with eight scan drivers, X-board, SMPS, logic, and address buffer. The X-electrodes are commonly connected to the X-board to allow the sustain pulses to be simultaneously applied to the X electrodes, whereas the Y electrodes are individually separated to operate the scan procedure line-by-line during an address-period. The reset and sustain waveforms are generated in the Y-board, meanwhile, the scan procedure is carried out by the scan buffer in the scan driver, as shown in Fig. 2, where the scan driver uses the scan buffer to play a role in supplying the output signal to the Y board to provide the scan pulses line-by-line from the 1st to the 480th scan line for the scan procedure. As such, the connection of the scan driver to the Y board is a very important part of the overlap-scan procedure in the address-period. The SMPS and logic board also play a role in providing the necessary power to each board and generating the necessary signals for each board, while the address buffer plays a role in scanning the cell for the display in a sustain-period by applying the address pulse to the address electrodes when applying the scan pulses to the Y electrodes. Fig. 3 (a) shows the conventional scan pulses with constant scan times of T_{sc} applied to the first three scan lines, and the corresponding IR emissions when simultaneously applying the address pulses with an application of the scan pulses during an address period.

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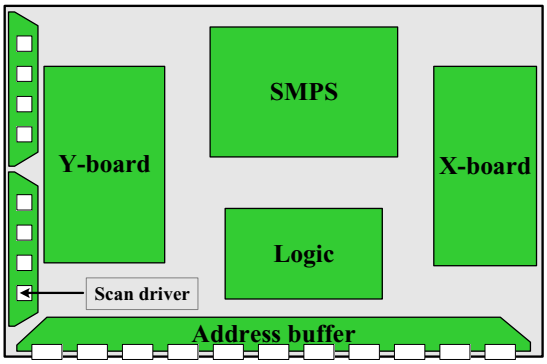


Fig. 2. Schematic diagram of back-plate of 42-in. plasma-TV comprised of Y-board with scan driver for scanning, X-board, SMPS, Logic, and Address buffer.

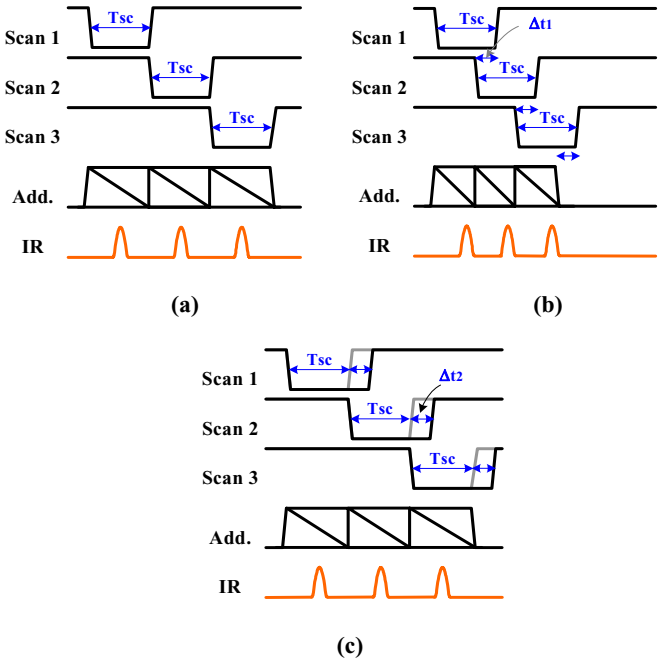


Fig. 3. (a) Conventional scan pulses with constant scan time of T_{sc} applied to first three scan lines and related IR emissions when applying address pulses during address period, (b) case 1: proposed overlap-scan pulses with constant scan times of T_{sc} and related IR emissions when applying address pulses during address period, and (c) case 2: proposed overlap-scan pulses with increased scan times of $T_{sc}+\Delta t$ and related IR emissions when applying address pulses during address period.

In this case, the width of the scan pulse is identical to that of the address pulse. Consequently, the total scan time can be determined by multiplying the 480 lines with the scan time T_{sc} per scan pulse. Fig. 3 (b) shows that the scan pulse overlaps with the previous scan pulse by Δt_1 when shifting the scan pulse to the left, where Δt_1 is the discharge delay time, *i.e.* the formative time lag. The scan pulse width of T_{sc} in Fig. 3 (b) is the same as that in Fig. 3 (a), yet the scan time can be reduced by Δt_1 per scan line by overlapping the scan pulses in the manner seen in Fig. 3 (b). As a result, in the case of overlapping the scan pulse, as shown in Fig. 3 (b), the total reduced scan time is $\Delta t_1 \times 480$ [lines], meaning that the driving waveform in Fig. 3 (b) is the scan waveform for a high-speed address. In contrast, Fig. 3 (c) shows that the scan pulse overlaps with the subsequent scan pulse when increasing the scan pulse to the right by Δt_2, where Δt_2 is also the discharge delay time, *i.e.* the formative time lag. Unlike the overlap-scan in Fig. 3 (b), the scan pulse width in Fig. 3 (c) is $T_{sc} + \Delta t_2$ per scan pulse, which is longer than that of the conventional case in Fig. 3 (a). However, the total scan time in Fig. 3 (c) does not increase in comparison with that in Fig. 3 (a) due to the overlap of the scan pulses for Δt_2. Instead, the scan pulse width in Fig. 3 (c) is increased by Δt_2 per scan pulse, thereby facilitating stable wall charge accumulations. As such, in the case of overlapping the scan pulses in the manner shown in Fig. 3 (c), the address voltage can be lowered without an additional increase in the scan time per scan line, meaning that the driving waveform in Fig. 3 (c) is the scan waveform for a low address voltage. In this paper, the two types of scan pulse shown in Figs. 3 (b) and (c) are the proposed waveforms for a high-speed and low address voltage, respectively. However, a conventional scan driver can not overlap the proposed scan waveforms in Figs. 3 (b) and (c), as the ensuing scan pulse can only be generated after the scan pulse falls down completely. Consequently, a new type of scan driving method is needed to generate the proposed overlap-scan waveforms.

III. Result and Discussion

Figs. 4 (a) and (b) show a schematic diagram of two wiring methods for providing the signals for scan pulses from the scan drivers to the Y-board for (a) the conventional and (b) proposed overlap-scan waveforms. As shown in Fig. 4 (a), the overlap-scan waveforms cannot be realized with the conventional wiring method, as the pins of the scan driver ICs are successively connected to the Y-board of the PDP module. Thus, to realize the overlap-scan waveforms, all the scan lines from 1st to 480th lines are grouped into odd or even lines, plus the total eight scan drivers are also grouped into four odd scan drivers and four even scan drivers. As shown in Fig. 4 (b), the 1st line, *i.e.* scan line 1, is the 1st odd scan line, the 2nd line, *i.e.* scan line 2, is the 1st even scan line, the 3rd line, *i.e.* scan line 3, is the 2nd odd scan line, the 4th line, *i.e.* scan line 4, is the 2nd even scan line, and so on. Thus, the total 480 scan lines consist of 240 odd scan lines and 240 even scan lines, where the odd and even scan lines are alternately located. Plus, the 1st odd scan driver is connected to the pins of the first sixty odd scan lines in the Y-board, while the 1st even scan driver is linked to the pins of the first sixty even scan lines located between the odd scan lines in the Y-board, as shown in Fig. 4 (b). Fig. 5 shows an operational block diagram of the 1st odd (even) scan driver for generating the overlap-scan waveform [5]. For the input signals in Fig. 5, the clock (*clk*) signal determines the application time of the scan pulse, whereas the blank (*blk*) signal determines the scan pulse width. In Fig. 5, the shift register plays a role in moving the output signal to the next scan line whenever the input signal, clk is given. Figs. 6 (a)

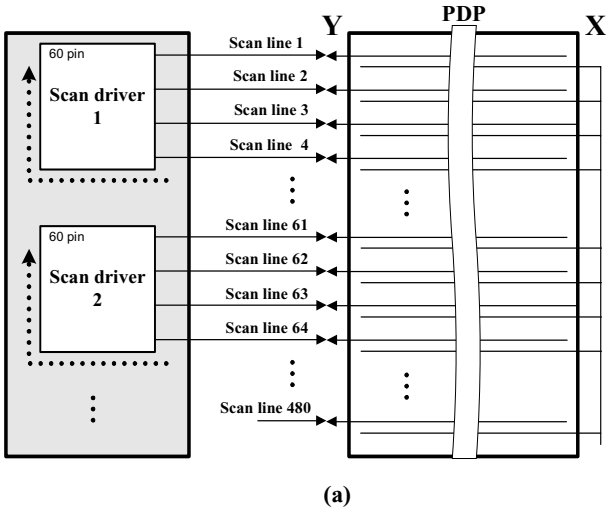


Fig. 4. Schematic diagram of wiring methods for overlap scan waveform.

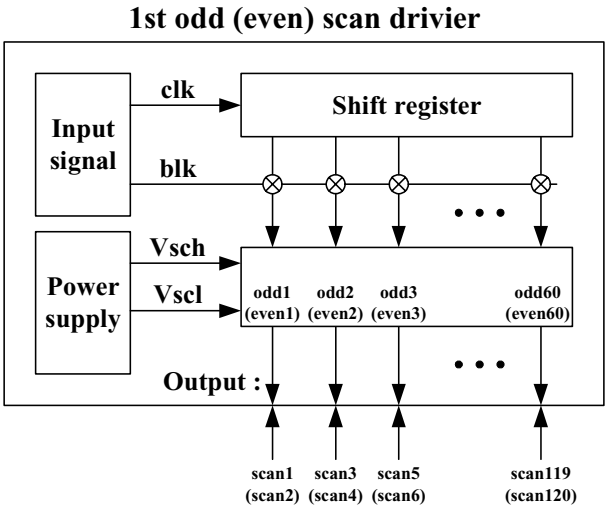


Fig. 5. Operational block diagram of 1st odd (even) scan driver for generation of overlap-scan waveforms.

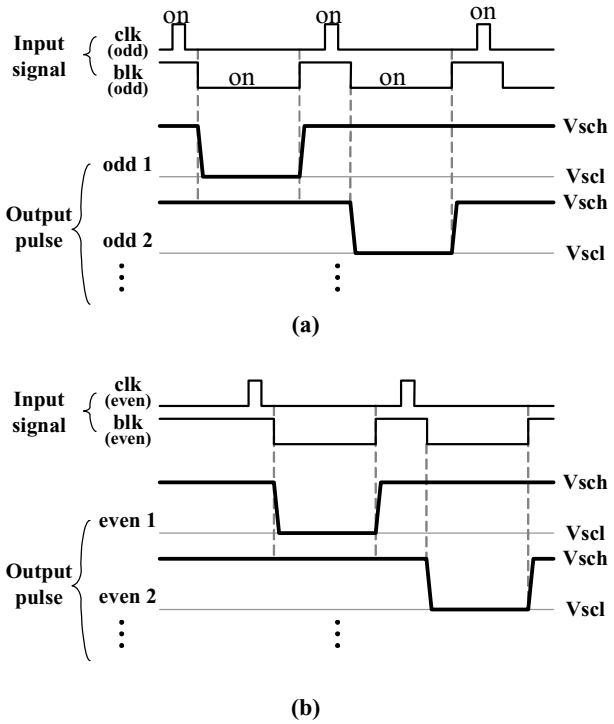


Fig. 6. Output pulse for generating overlap-scan waveforms according to input signals, *clk*, and *blk*.

and (b) show the output pulses generated according to the type of input signal, *clk* or *blk*, given from the 1st odd and even scan drivers, respectively. As shown in Fig. 6 (a), when the first *clk* signal is in an on-state, the corresponding scan voltage applied to the first odd scan line (scan 1) of the 60 scan lines is changed from the high scan voltage (V_{sch}) to the low scan voltage (V_{scl}). The low scan voltage (V_{scl}) then remains constant until the *blk* signal is in an on-state (low level), meaning that the scan pulse width is determined by the input signal, *blk*. Then, when the *blk* signal is transited from an on-state to an off-state (high level), the scan voltage is changed from the low scan voltage (V_{sch}) to the high scan voltage (V_{scl}), as shown in Fig. 6 (a). When the next *clk* signal is in an on-state, the corresponding scan voltage applied to the second odd scan line (scan 3) of the 60 scan lines is changed from the high scan voltage (V_{sch}) to the low scan voltage (V_{scl}). In a similar manner to the previous signal, the low scan voltage (V_{scl}) then remains constant until the *blk* signal is in an on-state. Fig.7 shows the overlapped output scan pulse alternately applied to the odd and even lines according the input signals, *clk* and *blk*. Unlike the conventional case, a pair of input signals, *clk* and *blk* are generated per odd or even line, and the resultant output scan pulses are alternately overlapped between the odd and even lines, as shown in Fig. 7. The adjacent two scan pulses, as detected by an oscilloscope, are shown in Fig. 5. For the gradually bright image pattern in Fig. 6 (a), some weak discharge or a discharge fail was observed in several gray levels when applying the conventional driving waveform,

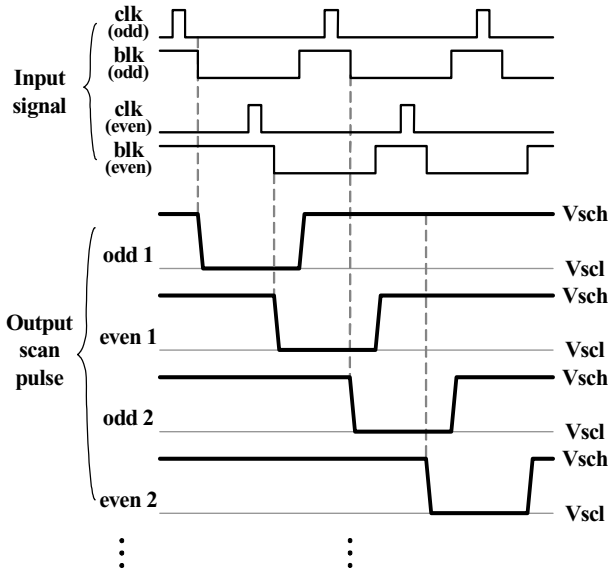


Fig. 7. Overlapped output scan pulses applied alternatively to odd and even lines according to input signals, *clk,and blk*.

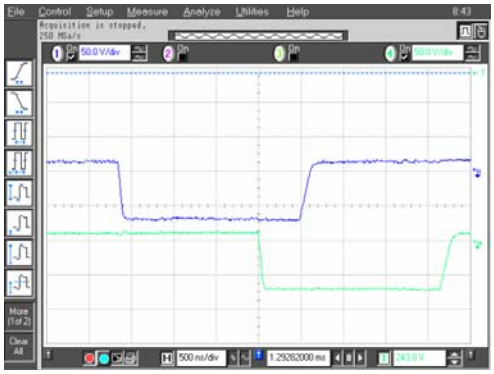


Fig. 8. Overlap-scan waveform (case 2 in Fig. 3 (c)) measured from 42-in. plasma-TV.

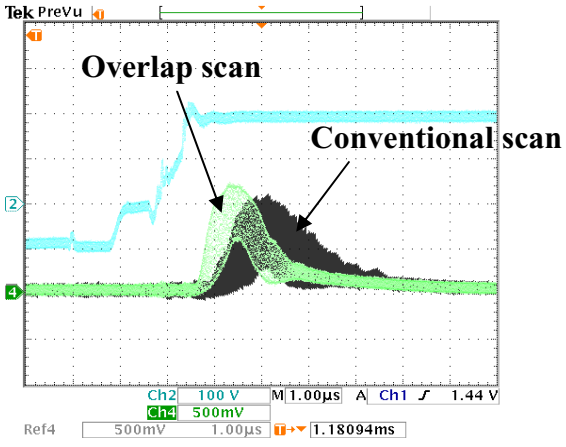


Fig. 9. Comparison of IR emission during first sustain discharge when applying conventional and proposed overlap- scan waveforms at address voltage of 70 V.

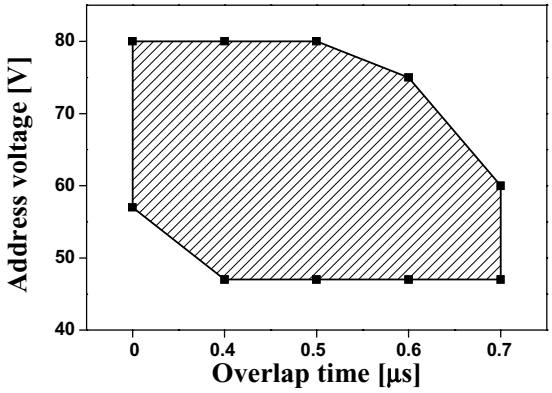
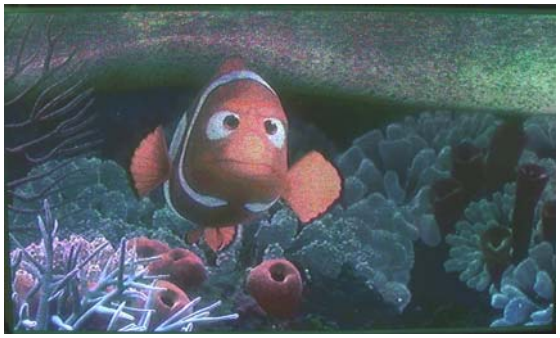
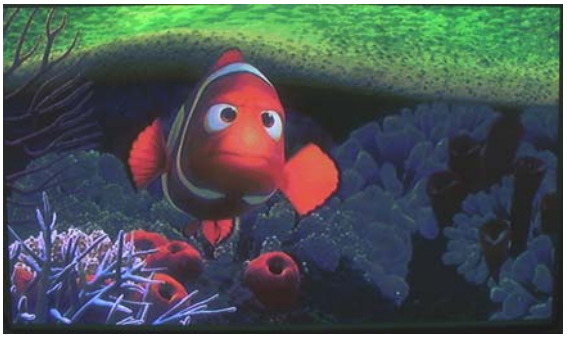


Fig. 10. Variations in address voltage margin relative to overlapped time, Δt_2 when adopting case 2 overlap-scan waveform in Fig. 3.

whereas the image pattern in Fig. 6 (b) shows a successful display when applying the overlap-scan driving waveform with an address voltage of 60 V and overlap scan time of 0.4 µs. Fig. 8 shows the overlap-scan waveform captured from the 42-inch plasma-TV, where the two adjacent scan pulses detected by an oscilloscope show the overlap-scan waveform. Fig. 9 shows the changes in the infrared (IR:828 nm) emission during the first sustain discharge when applying the conventional and proposed overlap-scan waveforms at an address voltage of 70 V. As shown in Fig. 8, the first sustain discharge after the total scanning procedure carried out using the proposed overlap-scan pulse was observed to be faster and more intense than that when using the conventional scan pulse. Therefore, this experimental result confirmed that the proposed overlap-scan pulse was able to intensify the address discharge without increasing the total scan time, thereby lowering the address voltage during the same scan period, or shortening the total scan time under the same address voltage conditions. Fig. 10 shows the variation in the address voltage relative to the overlap time, Δt_2 when adopting the case 2 of overlap-scan waveform in Fig. 3. With a zero overlap time, *i.e.* the conventional case, the minimum address voltage was about 57 V, whereas with an overlap time of over 0.4 µs, the minimum address voltage was reduced to about 47 V. The maximum address voltage margin was obtained with an overlap time of 0.4 or 0.5 µs, which was almost the same as the formative time lag. However, when the overlap time was longer than the formative time lag, a misfiring discharge occurred, which reduced the address voltage margin, as shown in Fig. 10. Figs. 11 (a) and (b) show the gradually bright image patterns on the 42-in. plasma-TV when the images were displayed using (a) the conventional scan circuit and (b) the proposed overlap-scan circuit providing an overlap-scan pulse. As shown in Fig. 11 (a), some weak discharges or discharge fails were observed in several gray levels when applying the conventional scan waveform. However, the image patterns in Fig. 11 (b) revealed a successful image without any weak discharge or discharge fail when applying the overlap-scan waveform.



(a)



(b)

Fig. 11. Image patterns on 42-in. plasma-TV at address voltage of 60 V and overlap scan time of 0.4 μs: (a) image displayed through conventional scan circuit, and (b) image displayed through proposed overlap-scan circuit providing case 2 overlap-scan waveform in Fig. 3 (c).

IV. CONCLUSION

A new overlap-scan circuit that enables high-speed or low data voltage scanning by overlapping the scan pulses during an address-period is proposed for a 42-in. plasma-TV. For the overlap between the scan pulses, the proposed overlap-scan circuit consists of three odd and three even drivers that alternately provide the scan pulses to the odd and even scan lines among the 480 scan lines, respectively. The proposed overlap-scan circuit can perform high-speed scanning by reducing the total scan time using the overlap between the scan pulses with constant scan pulse times. In addition, the proposed overlap-scan circuit can also perform low voltage scanning by lowering the address voltage using the overlap between the scan pulses with increased scan pulse times.

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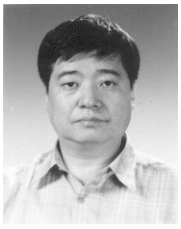

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